

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-307US1	Application No. 10/069,805
<b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary)		Applicant Gilbert Wolrich et al.	
		Filing Date November 7, 2002	Group Art Unit 2183
(37 CFR §1.98(b))			

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Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
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							Yes	No
/DJH/	DQ	0 130 381	01/1985	Europe				
	DR	0 463 855	01/1992	Europe				
	DS	0 476 628	03/1992	Europe				
	DT	0 696 772	02/1996	Europe				
	DU	WO03/019399	03/2003	WIPO				
/DJH/	DV	WO03/085517	10/2003	WIPO				

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/DJH/	DW	"HART, Field Communications Protocol, Application Guide", Hart Communication Foundation, pp. 1-74, (1999).
/DJH/	DX	Bowden, Romilly, "What is HART?" Romilly's HART® and Fieldbus Web Site, 3 pages, (1997). <URL: <a href="http://www.romilly.co.uk/whathart.htm">http://www.romilly.co.uk/whathart.htm</a> >

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/DJH/	DY	Cheng, et al., "The Compiler for Supporting Multithreading in Cyclic Register Windows", <i>IEEE</i> , pp. 57-62, (1996).
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	EA	Heuring et al., <i>Computer Systems Design and Architecture</i> , Reading, MA, Addison Wesley Longman, Inc., pp. 174-176 and 200, (1997).
	EB	Heuring et al., <i>Computer Systems Design and Architecture</i> , Reading, MA, Addison Wesley Longman, Inc., pp. 38-40, 143-171, and 285-288, (1997).
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	ED	Hirata, H., et al., "An Elementary Processor Architecture with Simultaneous Instruction Issuing from Multiple Threads", <i>Proc. 19th Annual International Symposium on Computer Architecture, ACM &amp; IEEE-CS</i> , 20(2):136-145, May 1992.
	EE	Intel, "IA-64 Application Developer's Architecture Guide," Rev.1.0, pp. 2-2, 2-3, 3-1, 7-165, C-4, and C-23, May 1999.
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	EG	Koch, G., et al., "Breakpoints and Breakpoint Detection in Source Level Emulation", <i>Proc. 19th International Symposium on System Synthesis (ISSS '96)</i> , <i>IEEE</i> , pp. 26-31 (1996).
	EH	Moors, et al., "Cascading Content-Addressable Memories", <i>IEEE Micro</i> , 12(3):56-66 (1992).
	EI	Okamoto, K., et al., "Multithread Execution Mechanisms on RICA-1 for Massively Parallel Computation", <i>IEEE - Proc. Of PACT '96</i> , pp. 116-121 (1996).
	EJ	Patterson, et al., <i>Computer Architecture A Quantitative Approach</i> , 2nd Ed., Morgan Kaufmann Publishers, Inc., pp. 447-449, (1996).
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	EL	Philips ED - Philips Components: "8051 Based 8 Bit Microcontrollers, Data Handbook Integrated Circuits, Book IC20", 8051 Based 8 Bit Microcontrollers, Eindhoven, Philips, NL, pp. 5-19 (1991).
	EM	Probst et al., "Programming, Compiling and Executing Partially-Ordered Instruction Streams on Scalable Shared-Memory Multiprocessors", <i>Proceedings of the 27th Annual Hawaiian International Conference on System Sciences</i> , <i>IEEE</i> , pp. 584-593, (1994).
	EN	Quammen, D., et al., "Flexible Register Management for Sequential Programs", <i>IEEE Proc. of the Annual International Symposium on Computer Architecture</i> , Toronto, May 27-30, 1991, vol. SYMP. 18, pp. 320-329.
	EO	Ramsey, N., "Correctness of Trap-Based Breakpoint Implementations", <i>Proc. of the 21st ACM Symposium on the Principles of Programming Languages</i> , pp. 15-24 (1994).
	EP	Steven, G.B., et al., "ALU design and processor branch architecture", <i>Microprocessing and Microprogramming</i> , 36(5):259-278, October 1993.
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/DJH/	AD	7,181,594	02/2007	Wilkinson, III et al.			
/DJH/	AE	7,191,309	03/2007	Wolrich et al.			
	AF						
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	AI						
	AJ						
	AK						

Foreign Patent Documents or Published Foreign Patent Applications								
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							Yes	No
	AL							
	AM							
	AN							
	AO							
	AP							

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	AT	

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